#17 Appeal Brief (2) 11/24/03

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IN RE APPLICATION OF: Braddock

Examiner: KANG

SERIAL NO: 09/636,484

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TITLE: INTEGRATED TRANSISTOR DEVICES

TO: ASSISTANT COMMISSIONER OF PATENTS

37 CFR 1.192(b)(2)(ii) REQUEST TO REINSTATE THE APPEAL AND SUPPLEMENTAL APPEAL BRIEF

Sir: In response to the Notification of Non-Compliance with 37 CFR 1.192(c) mailed October 21, 2003, further to the appeal brief 37 CFR 1.116 amendment after appeal and declaration filed April 29, 2003 and re-filed September 25, 2003, which was in responsive to the non-final office action dated 1/30/2003, the applicant maintains the appeal and the traversal of the restriction requirement, and complies the requirement in the Notification mailed October 21, 2203 with this revised Brief. The applicant has filed a separate paper objecting to the Notification of Non-Compliance with 37 CFR 1.192(c) mailed October 21, 2003 requesting that Notification be vacated and that the appeal brief filed April 25, 2003 be reinstated.

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TRAVERSAL OF THE ELECTION REQUIREMENT - CLAIMS 53-55

The board should note that the applicant maintains the traversal of the restriction requirement of claims 53-55 and that a petition requesting withdrawal of that requirement is pending. The applicant presumes for this appeal that the petition has been granted and that claims 53-55 are not withdrawn in order to expedite prosecution. In that regard, claim 53 should be allowable over the prior art applied to rejected claims 36 and 38 for the reasons presented for claim 36. Claims 54 and 55 recite limitations not addressed by the examiner and therefore should be allowable over the art applied by the examiner for that additional reason.

37 CFR 1.193(b)(ii) SUPPLEMENTAL APPEAL BRIEF

I. **37 CFR 1.192(a)**

This supplemental brief is being filed within 3 months from the examiner's 37 CFR 1.193(b)(2) reopening or prosecution after appeal. The notice of appeal and fee for the notice of appeal were filed with the original brief. The supplemental brief is filed in triplicate. The supplemental brief sets forth the authorities and argument the applicant will rely upon in the appeal.

II. **37 CFR 1.192(b)**

The appeal is timely and should not be dismissed.

III. **37 CFR 1.192(c)**

A. **Real Party in Interest**

The real party in interest is Osemi, Inc., which is wholly owned by David Braddock, the named inventor.

B. **Related Appeals and Interferences**

There are no related appeals or interferences.

C. **Status of Claims**

Claims 1-26 and 36-55 are pending. Claims 53-55 stand withdrawn. The applicant is disputing the withdrawal of claims 53-55 via a petition previously filed. Claims 1-26, 37, and 39-52 stand allowed. Claims 36 and 38 stand rejected.[1] New claims 56 and 57 and an amended version of claim 36 were presented in a 37 CFR 1.116 amendment filed with the Brief filed April 129, 2003.

While the office action is not final, the applicant exercises the right to maintain the appeal pursuant to 37 CFR 1.193(b)(ii), and 37 CFR 1.116 expressly applies to "Amendments after final action or appeal". Accordingly, the examiner has the right to not enter the amendment. However, the amendment and associated evidence show clearly and convincingly that the rejections of claims 36 and 38 are improper. Accordingly, I strongly urge the examiner to enter the amendment and allow claims 36 and 38 as well as the newly presented dependent claims 56 and 57.

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[1]If the examiner withdraws the restriction requirement prior to decision on appeal, then claims 53-55 will be pending and not withdrawn, and either allowed or rejected. This brief addresses the contingency in which those claims are rejected on the same grounds as claims 36 and 38.

Clean copies (1) of claims as they now stand and (2) as they will stand if the examiner enters the amendment are attached as an appendix in case the examiner decides to exercise his discretion to enter the amendment instead of or in addition to filing an Examiner's Answer. See 37 CFR 1.193(1) and (b)(2).

D. **Status of amendments**

An amendment filed pursuant to 37 CFR 1.116/37 CFR 1.193(a)(2) was filed April 29, 2003 and stands un-entered as of October 23, 2003.

E. **Summary of the Rejected Inventions Under Appeal with Reference to Page and Line Numbers and Drawings**

The rejected inventions provide (claim 36) an enhancement mode metal-oxide-compound semiconductor field effect transistor (Fig. 1 element 10) comprising:

a compound semiconductor wafer structure (Fig. 1 element 13 and page 6 line 8) having an upper surface;

a gate insulator structure (Fig. 1 element 30 and page 6 line 13) positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode (Fig. 1 element 17 and page 6 line 20) positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode (Fig. 1 elements 21, 22; specification page 6 fourth line from bottom) ; and

source and drain ohmic contacts (Fig. 1 elements 19, 20 and page 6 fifth line from bottom) positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer (Fig. 1 element 15 and page 5 lines 19-20), said layer being positioned on said upper surface;

a substrate (Fig. 1 element 11 and page 6 line 12) on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer (page 5 third line from bottom).

If the after appeal amendment is entered, then claim 36 defines "a Al_xIn_{1-x} As, $In_yGa_{1-y}As$, or InP layer" instead of an Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer.

The claim 38 invention also provides that "said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit."

F. **Issues**

I. Whether the rejections of claim 36 as obvious in view of USP 5,945,718 to Passlack and the USP to Kikkawa should be reversed.

II. Whether the rejections of claim 38 as obvious in view of USP 5,945,718 to

Passlack should be reversed.

G. Groupings of Claims

The claims do not stand or fall together.
Group 1 - Claim 36
Group 2 - Claim 38
If entered prior to decision on appeal, each one of claims 53-57 define a separate group, groups 3-8, respectively.
The claims do not stand or fall together.

H. Argument (Reasoning)

1. Why Claims 36 and 38 Comply with 35 USC 103

In rejecting claims 36 as obvious over Passlack in view of Kikkawa, the examiner now states that:

> Passlack et al. teach an enhancement mode metal-oxide-compound semiconductor field effect transistor comprising (Fig. 1):
> A compound semiconductor wafer structure (12) having an upper surface' [sic] a gate insulator structure (14) positioned on upper surface of said compound semiconductor wafer structure; a gate electrode (17) positioned on upper surface of said gate insulator structure layer; source (21) and drain (22) ion implants self-aligned to the gate electrode; and source and drain ohmic contacts (19 & 20) positioned on ion implanted source and drain areas, wherein said compound semiconductor wafer structure comprises a AlGaAs (23) and InGaAs (24) layers positioned on said upper surfaces; and a substrate (11) on which resides said compound semiconductor wafer structure. See also Col. 2, line 65 - Col. 4, line 4.
> Passlack teaches a GaAs substrate instead of [an] InP substrate. However, Kikkawa teaches that one may use InP for the substrate in place of GaAs (Col. 16, lines 5-9). Therefore, it would have been obvious in the art at the time the invention was made to substitute [the] GaAs substrate of Passlack with InP substrate as taught by Kikkawa, since both GaAs and InP exhibits faster and more optimized speed/power performance.
> Furthermore, one of ordinary skill in the art would have recognized that GaAs and InP would have worked equally as well as a substrate material for various high speed devices, such as MISFET, HEMPT or HBT. [Office action mailed 1/30/3003 page 5 lines 3-22.]

In rejecting claims 38 as obvious over Passlack, the examiner now states that:

> Passlack teaches an enhancement mode metal-oxide-compound

semiconductor field effect tranasistor comprising (Fig. 1):

a compound semiconductor wafer structure (12) having an upper surface; a gate insulator structure (14) positioned on said upper surface; a gate electrode (17) positioned on upper surface of said gate insulator structure layer; source (21) and drain (22) ion implants (19 and 20) positioned on ion implanted source and drain areas wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer (InGaAs, 24). See also Col. 2, line 65 - Col. 4 line 4.

Passlack does not show in Fig. 1 that transistor is integrated together with similar and complementary devices to form complementary metal-oxide compound semiconductor integrated circuit. However, it is well known to form MOS transistors (CMOS) which are used generally in various devices of LSI constitution including memory LSIs and logic LSIs since they have advantageous features of low power and high speed operation. The advantageous [sic] of complementary metal oxide semiconductor devices are well known in the art. Note that Passlack also teaches complementary GaAs devices exhibit optimum speed/power performance and efficiency at low supply voltage of 1 V and below (Col. 1 lines 18-24.) .. that complementary GaAs exhibits optimum speed/power performance and efficiency at a low supply voltage of 1 V and below (see Col. 1, lines 22-24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate transistor together with complementary metal-oxide semiconductor integrated circuit because of the well known advantages of CMOS configurations. [Office action page 6 line 15 to page 7 line 17.]

In reply, the applicant disagrees with the examiner's statements of fact and conclusions of law. Specifically, the applicant submits for the reasons presented below (1) that Passlack does not disclose a gate insulator structure and (2) there is no motivation to modify Passlack in view of Kikkawa by substituting Passlack's substrate with Kikkawa's substrate.

As factual matters, Passlack's Ga2O3 is not insulating and the structure of layers above Passlack's GaAs substrate could not be grown on Kikkawa's InP substrate. These facts are inconsistent with the obviousness conclusions reached by the examiner. Therefore, the examiner's conclusions are not supported by substantial evidence.

Moreover, the examiner's conclusion that Kikkawa teaches the equivalency of InP and GaAs substrates is inconsistent with additional facts noted herein and also contrary to an interpretation of Kikkawa that is consistent with all facts of record and additional facts supported by evidence filed herewith.

a. **Additional Facts**

The following additional facts and conclusions are supported by the second 37 CFR 1.132 declaration of the inventor, David Braddock, and attachments 1-3, all filed with this substitute

appeal brief on April 29, 2003.

1. There is no AlGaAs composition for which lattice matching exists with InP. The lattice constants of InP and AlGaAs, at any composition of AlGaAs, are so far apart that epitaxially growth of the AlGaAs in InP is impossible. Therefore, AlGaAs can not be grown epitaxially on InP. These facts are well known in the art. Non-epitaxially grown AlGaAs on InP has no device potential and therefore no utility of which David Braddock is aware.

2. Even for a composition of $In_xGa_{1-x}P$ containing as low as one percent GaP, $In_xGa_{1-x}P$ does not lattice match to an InP substrate. Therefore, InGaP cannot be grown epitaxially on InP with low defect densities. These facts are well known in the art. Compositions of less then one percent GaP in $In_xGa_{1-x}P$, wherein lattice matching may be possible, on InP, have no device potential and therefore no utility of which David Braddock is aware . InGaP grown non-epitaxially on InP has no device potential and therefore no utility of which David Braddock is aware. Therefore, $In_xGa_{1-x}P$ on InP has no utility of which David Braddock is aware.

3. The applied Passlack patent teaches using only AlGaAs or InGaP lattice matched to GaAs. The applied Passlack patent does not mention InP substrates. Dr. Braddock presumes that Passlack's failure to mention InP substrates is at least because Dr. Passlack knew that his AlGaAs and InGaP devices grown on an InP substrate would not grow epitaxially on InP and therefore could not produce a useful device.

3a. In a telephone conference with counsel on April 18, 2003, Dr. Braddock reviewed the office action and the outstanding rejections against this application. During that review Dr. Braddock recognized that his claim 36, as amended, claimed some inoperative embodiments, in that claim 36 claimed alternatives of an AlGaAs heterostructure or an InGaP heterostructure grown on InP. Dr. Braddock's specification for this application, in the summary of the invention, states the following for the InP substrate inventions:

> In another preferred embodiment, the compound semiconductor heterostructure comprises an $In_yGa_{1-y}As$, $Al_xIn_{1-x}As$, and InP compound semiconductor heterostructure and n-type and/or p-type charge supplying layers which are grown on an InP substrate, and a refractory metal gate of W, WN, or WSi, self aligned donor (n-channel FET) or acceptor (p-channel FET) implants, and source and drain ohmic contacts.

That passage defines $Al_x\underline{In}_{1-x}As$, not $Al_x\underline{Ga}_{1-x}As$, as an alternative composition of the heterostructure on an InP substrate. That passage does not define InGaP as an alternative composition of the heterostructure on an InP substrate. Nevertheless, the rejection of claim 36 as unpatentable for obviousness is still improper because the subject matter defined by claim 36 is in fact not obvious. The 37 CFR 1.116 amendment submitted April 29, 2003 proposes changes to claim 36, which, if entered, would correct the defects noted above.

4. It is now known that stoichiometric Ga2O3 is an *n type semiconductor*, not an insulator. It has room temperature residual n type conductivity on the order of 10^{16} per cubic centimeter. That conductivity is much larger than the conductivity of insulating materials used as gate insulators. Materials used as gate insulators generally must have conductivities of *less than* 10^{12} per cubic centimeter. Accordingly, stoichiometric Ga2O3, which is what the Passlack patent

teaches, is not useful for performing the function of a gate insulator.

5-5a. At the time Passlack filed for the applied Passlack patent, Dr. Braddock believes that Passlack did not know that stoichiometric Ga2O3 had a relatively large residual conductivity. Dr. Braddock speculates that Passlack filed for the Passlack patent assuming that residual conductivity of Ga2O3 was caused by defects, vacancies, or impurities and therefore Passlack thought that conductivity could potentially be reduced to a level at which his Ga2O3 would be commercially useful as a gate insulator.

5b. Dr. Passlack has recently first authored a book chapter regarding Gallium Oxide on GaAs, co-authored with Dr. Braddock and others.[2] In that chapter, Dr. Passlack admits that, even though stoichiometry of Ga2O3 can be maintained, Ga2O3's inherently conductive nature cannot be eliminated. Dr. Passlack's own book chapter discusses that conductivity of Ga2O3 is as high as 10E18, and that the specific resistivity is always low relative to an insulator. See section 4.3, page 347. Moreover, Passlack also has another patent, 6,094,295, wherein he identified Ga2O3 as a UV transparent conducting material.[3] For example, see the abstract of 6,094,295. Thus, the implication that the examiner draws from the applied Passlack patent, which is that Ga2O3 can form an insulating layer, and therefore that it can form a gate insulating layer, is clearly incorrect.

6. Moreover, the devices disclosed in the applied Passlack patent are not commercially useful and have no practical utility due to their reliance on Ga2O3. As Dr. Braddock states it, "the Passlack device is not commercially useful and would not have any practical utility. I state this because the Ga2O3 oxide leaks just as badly or worse than a standard compound semiconductor HEMT (or PHEMT) that utilizes gate metal directly on top of an AlGaAs top layer. The metal on the AlGaAs layer forms a Schottky-barrier to current flow at the gate of the transistor. In the case of Passlack, the Ga2O3 can be so highly conducting (e.g. 10E18cm-3 conductivity) that the gate metal on Passlack's MOSFETs will form Ohmic contacts at the gate (and thus have huge gate leakage). Thus, Passlack's MOSFET devices that utilize Ga2O3-on-GaAs would have no practical utility over the prior art (i.e. standard HEMTS and PHEMTs) over which Passlack has obtained a patent."

7. The Passlack patent does not disclose a gate insulator. Instead, the Passlack patent discloses:

> The FET includes a *stoichiometric Ga2O3 gate oxide layer* positioned on upper surface of a compound semiconductor wafer structure. [Col. 2 lines 45-47; emphasis supplied.]

b. **Reasoning**

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[2]A copy of chapter 12, entitled "Gallium Oxide on Gallium Arsenide: Atomic Structure, Materials, and Devices", is attachment 1 to the Brief filed April 29, 2003. Chapter 12 is either published or scheduled for publication in "Gallium Oxide on Gallium Arsenide: Atomic Structure, Materials, and Devices" in III-V Semiconductor Heterostructures: Physics and Devices, edited by W.Z. Cai, Transworld Research Publisher, Kerala, India (2003).

[3]A copy of 6,094,295 to Passlack is attachment 2 to the Brief filed April 29, 2003.

Obviousness requires both a specific teaching suggesting the proposed motivation and a reasonable expectation of success. In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

"Where claimed subject matter has been rejected as obvious in view of a combination of prior art references, a proper analysis under § 103 requires, inter alia, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. See In re Dow Chemical Co., 837 F.2d 469, 473, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988). Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure. Id." In re Vaeck, ___ F.3d ___, 20 USPQ2d 1438 (Fed. Cir. 1991).

Neither is present in this case.

i. **No motivation to combine**

8. There is no motivation in the art to substitute InP for the GaAs substrate used by Passlack, for two reasons. First, there is no specific teaching or suggestion of such a modification of Passlack's teachings. Second, it is well known that such a substitution would prevent epitaxial growth of either one of the AlGaAs and InGaP materials that Passlack discloses are epitaxially grown in his structure on GaAs.

8a. The lattice constants of InP and AlGaAs, at any composition, are so far apart that epitaxially growth of the AlGaAs is impossible.

8b. The lattice constants of InP and GaP are so far apart that only less than a one percent solid solution in GaP in InP can be grown epitaxially on InP, and there are no known uses for such a low concentration solid solution of InGaP grown epitaxially on an InP substrate.

8c. The examiner asserts now that Kikkawa provides a teaching to substitute an InP substrate for the GaAs substrate of Passlack. Not so!

8d. Kikkawa describes a method and device structure for improving the contact resistance of p-type MISFET devices fabricated in GaAs-compatible materials systems. The materials of the layers that Kikkawa describes possess lattice constants similar to or slightly strained from GaAs. These materials all have lattice constants close enough to GaAs so that they can be grown epitaxially on a GaAs substrate.

8e. Kikkawa does not describe a compound semiconductor structure or transistor that would have any possibility of being grown epitaxially on an InP substrate. Depositing any of the structures described in the embodiments of Kikkawa on an InP substrate will result in the

deposited layers being amorphous. This collection of amorphous layers would result in a transistor-like structure, in the sense that its macroscopic shape would look like a transistor, but that transistor-like structure would not function as a transistor. Thus, InP could not be substituted for the GaAs substrate for any embodiment disclosed in Kikkawa.

8f. Kikkawa does not facially suggest use of an InP substrate. Instead, he states that:

> In the present embodiment, the material of the channel layer 54 acting also as the etching stopper is not limited to InGaAs but other materials such as InGaAsP or InGaP may also be used. Further, one may use InP for the substrate 51 in place of GaAs. The barrier layer 55, in turn, may be formed of GaAsSb or AlGaAsSb. [Column 16 lines 5-10; emphasis added.]

8g. However, it appears that, in context, and based upon that fact that neither AlGaAs nor InGaP lattice matches to InP, Kikkawa is suggesting a completely alternative structure to the GaAs substrate structure of the embodiment discussed up to column 16 line 5. That is, it appears that Kikkawa is suggesting using Sb based layers on InP as opposed to AlGaAs or InGaP layers. This is (1) because certain compositions of the Sb based quaternary's noted by Kikkawa, which are GaAsSb or AlGaAsSb, do lattice matched to InP because they have similar enough lattice constant to InP and (2) because no substantial composition of Sb in GaAsSb can lattice match to a GaAs substrate. The fact that a GaAsSb composition can lattice match to InP is confirmed by Fig. 2 of Vurgaftman et al, "Band Parameters for III-V Semiconductors and Their Alloys", J. Appl. Phys. PP 5816-5875 (June 1, 2001).[4] Figure 2 shows a line connecting GaAs to GaSb indicating the existence of GaAsSb solid solution. That solid solution contains compositions having the same lattice constant as InP, as indicated by the fact that the line crosses on the x axis the lattice constant value for InP and therefore enabling lattice matching to InP. The fact that no substantial composition of Sb in a layer of GaAsSb will lattice match to GaAs is apparent from the relatively large lattice constant differences of GaAs and GaSb. Therefore, the only reasonable inference to draw from Kikkawa's reference to InP in combination with Sb based semiconductors is that a total replacement of all layers with InP and Sb based materials instead of merely replacing the GaAs substrate with InP. For all of these reasons, the examiner's interpretation of the teachings of Kikkawa are incorrect. Kikkawa does not suggest that GaAs and InP are equivalent or that they can be substituted for one another.

8h. Neither Passlack nor Kikkawa suggest substituting an InP substrate for the GaAs substrate of Passlack. Moreover, such a substitution would result in a non-functional device since (1) AlGaAs cannot be grown epitaxially on InP and (2) InGaP cannot (to an extent that could provide any useful properties) be grown epitaxially on InP. Since the teachings of Passlack and Kikkawa do not suggest combination, the rejection of claim 36 is improper and should be reversed.

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[4]A copy of Vurgaftman et al, "Band Parameters for III-V Semiconductors and Their Alloys", J. Appl. Phys. PP 5816-5875 (June 1, 2001) is attachment 3 to the Brief filed April 29, 2003.

ii. **The Proposed Combination is Not Subject Matter Defined by Any Claim**

The examiner's construction of the claims is improper since the examiner has not construed the meaning to one of ordinary skill in the art the of the claimed "gate insulator structure" based upon what is stated in the specification, as required by law.

> The written description must be examined in every case, because it is relevant not only to aid in the claim construction analysis, but also to determine if the presumption of ordinary and customary meaning is rebutted. See Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1250, 48 USPQ2d 1117, 1122 (Fed. Cir. 1988). The presumption will be overcome where the patentee, acting as his or her own lexicographer, has clearly set forth a definition of the term different from its ordinary and customary meaning. See In re Paulsen, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994); Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992). The presumption also will be rebutted if the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope. See Teleflex, 299 F.3d at 1324, 63 USPQ2d at 1380. [Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc., ___ F.3d ___, ___, ___ USPQ2d ___, ___ (Fed. Cir. Docket No. 02-1145, 4/11/03).]

9. Second, Passlack's stoichiometric Ga2O3 does not respond to the limitation defined in claims 36 and 38 of "a gate insulator structure." The first paragraph of the section of the specification of this application describing the invention defined the "gate insulator structure" recited in claims 36 and 38 as both electrically insulating and comprising at least two layers. That paragraph states in part:

> The present invention provides, among other things, a self-aligned enhancement mode metal-oxide-compound semiconductor FET. The FET includes *a gallium oxygen insulating structure that is composed of at least two distinct layers.* The *first layer is* most preferably more that 10 angstroms thick but less that 25 angstroms in thickness and *composed substantially of gallium oxygen compounds including but not limited to stoichiometric Ga_2O_3 and Ga_2O, and possibly a lesser fraction of other gallium oxygen compounds.* The *upper insulating layer in the gallium oxide insulating structure* is composed of an insulator that does not intermix with the underlying gallium oxygen insulating structure. This upper layer must possess excellent insulating qualities, and is most typically composed of gallium oxygen and a third rare earth element that together form a ternary insulating material. *Therefore the entire gallium oxide rare earth gate insulator structure is composed of at least two layers* and may contain a third intermediate graded layers that consists of a mixture of the upper insulating

material and the gallium oxygen compounds that compose the initial layer.

10. Please note that the specification was written by Dr. Braddock, the inventor, without advise of counsel, which explains in part the reference to two layers as "first layer" and an "upper insulating layer" to the extent that that lack of clarity and any other descriptions that lack complete clarity cause the panel any confusion.

11. The specification contains specific references to "gate insulator structure" or the equivalent "gate insulating structure" all of which are consistent with a multi layer structure that is insulating to the extent necessary to form a useful gate insulator. See the recitations:

> A refractory metal gate electrode is preferably positioned on the upper surface of the gate insulator structure layer. [Page 5 lines 10-12.]
>
> Together the lower gallium oxide compound layer and the second insulating layer form a gallium oxide gate insulating structure. [Abstract.]
>
> The gallium oxide gate insulating structure and underlying compound semiconductor gallium arsenide layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14). [Abstract.]

Therefore, the proposed combination does not result in subject matter defined by claim 36. Therefore, the rejection of claim 36 should be reversed.

12. Third, Passlack does not disclose a gate insulator. The teachings of Passlack do not enable one skilled in the art to form a structure containing a commercially useful device because the conductivity of the *stoichiometric Ga2O3 gate oxide layer* taught by Passlack is too high to be useful. Passlack does not teach one or ordinary skill in the art that the conductivity of the *stoichiometric Ga2O3 gate oxide layer* taught by Passlack is too high to be useful. Moreover, Passlack does not teach one of ordinary skill in the art how to make a gate insulating structure having low enough conductivity to be useful.

Therefore, the proposed combination does not result in subject matter defined by claim 36. Therefore, the rejection of claim 36 should be reversed.

IV. Claim Groups

A. Group 1 - Claim 36

The obviousness rejection of claim 36 should be reversed because Passlack and Kikkawa patent do not suggest any modification of Passlack to define a "substrate [that] includes a InP based semiconductor wafer" and because the proposed combination does not define the "gate insulator structure."

B. Group 2 - Claim 38

The obviousness rejection of claim 38 should be reversed because the Passlack patent does suggest a "gate insulator structure," as claimed.

C. **Claims 53-55**

If considered on appeal, claim 53-55 are non-obvious over the applied Passlack patent for the reasons presented for claim 36.

D. **Claim 54**

If considered on appeal, claim 54 is non-obvious over all applied prior art for the additional reason that it recites "rapid thermal annealing said structure in UHV."

E. **Claim 55**

If considered on appeal, claim 55 is non-obvious over all applied prior art for the additional reason that it recites "rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade."

F. **Claim 56**

If considered on appeal, claim 56 is non-obvious over all applied prior art for the additional reason that it recites "an InP upper spacer layer."

G. **Claim 57**

If considered on appeal, claim 57 is non-obvious over all applied prior art for the additional reason that it recites "said compound semiconductor wafer structure is formed from a layer comprising InGaP."

Respectfully Submitted,

31518
PATENT TRADEMARK
OFFICE

10/27/03
Date

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APPENDIX 1 - CLAIMS REJECTED AND UNDER APPEAL WITHOUT ENTRY OF 37 CFR 1.116 AMENDMENT FILED WITH THIS SUPPLEMENTAL APPEAL BRIEF

Claims 36 and 38 read as follows:

36. (Previously Amended) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on said upper surface;

a substrate on which resides said compound semiconductor wafer structure; and

wherein said substrate includes a InP based semiconductor wafer.

38. A complementary metal-oxide compound semiconductor integrated circuit comprising an enhancement mode metal-oxide-compound semiconductor field effect transistor, said transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on said upper surface;

a gate electrode positioned on said upper surface;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer;

wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$; and

and wherein said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit.

53. A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

54. The method of claim 53 comprising rapid thermal annealing said structure in UHV.

55. The method of claim 54 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.

APPENDIX 2 - CLAIMS REJECTED AND UNDER APPEAL WITH ENTRY OF 37 CFR 1.116 AMENDMENT FILED WITH THIS SUPPLEMENTAL APPEAL BRIEF

- - - DELETED IN RESPONSE TO NOTIFICATION OF NON-COMPLIANCE MAILED 10/21/2003 - - -

APPENDIX 3 - ALL PENDING CLAIMS AS THEY STAND AND ALTERNATIVELY SHOWING THEM IF THE 37 CFR 1.116 AMENDMENT IS ENTERED

- - - DELETED IN RESPONSE TO NOTIFICATION OF NON-COMPLIANCE MAILED 10/21/2003 - - -

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